Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A digital baseband (DBB) receiver for adjusting a ~~the~~ frequency domain response of at least one of ~~the~~ real and imaginary signal components of a wireless communication signal, the DBB receiver comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths, the digital HPFC module comprising:

a real signal input for receiving the real signal component;

a real compensated signal output for outputting a real compensated output signal;

a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

a first sample delay unit having an input and an output, the input of the first sample delay unit being connected to the output of the second adder;

a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the first sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module;

an imaginary signal input for receiving the imaginary signal component;

an imaginary compensated signal output for outputting an imaginary compensated output signal;

a third multiplier having first and second inputs and an output, the first input of the third multiplier for receiving the first compensation signal;

a fourth adder having first and second inputs and an output, the first input of the fourth adder being connected to the imaginary signal input of the digital HPFC module, and the output of the fourth adder being connected to the second input of the third multiplier;

a fifth adder having first and second inputs and an output, the first input of the fifth adder being connected to the output of the third multiplier;

a second sample delay unit having an input and an output, the input of the second sample delay unit being connected to the output of the second adder;

a fourth multiplier having first and second inputs and an output, the first input of the fourth multiplier for receiving the second compensation signal, the second input of the fourth multiplier being connected to the output of the second sample delay unit, to the second input of the fifth adder, and to the second input of the fourth adder; and

a sixth adder having first and second inputs and an output, the first input of the sixth adder being connected to the first input of the fourth adder, the second input of the sixth adder being connected to the output of the fourth multiplier, and the output of the sixth adder being connected to the imaginary compensated signal output of the digital HPFC module;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal path of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

Claim 2 (canceled)

3. (currently amended): The DBB receiver of claim 1 ~~claim 2~~ wherein a cutoff frequency, established by the analog real signal path HPF for the real signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

4. (currently amended): The DBB receiver of claim 1 ~~claim 2~~ wherein the gain of the high pass response of the real signal component frequency domain is

controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

5. (currently amended): The DBB receiver of claim 1 ~~claim 2~~ wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

6. (currently amended): The DBB receiver of claim 1 ~~claim 2~~ wherein the output of the first sample delay unit is subtracted from the real signal component via the first adder.

Claim 7 (canceled)

8. (currently amended): The DBB receiver of claim 1 ~~claim 7~~ wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

9. (currently amended): The DBB receiver of claim 1 ~~claim 7~~ wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

10. (currently amended): The DBB receiver of claim 1 ~~claim 7~~ wherein the output of the fourth ~~second~~ multiplier is subtracted from the imaginary signal component via the sixth ~~third~~ adder.

11. (currently amended): The DBB receiver of claim 1 ~~claim 7~~ wherein the output of the second sample delay unit is subtracted from the imaginary signal component via the fourth ~~first~~ adder.

12. (original): The DBB receiver of claim 1 wherein the digital HPFC module is selectively enabled or disabled.

13. (currently amended): A wireless transmit/receive unit (WTRU) for adjusting a ~~the~~ frequency domain response of at least one of ~~the~~ real and imaginary signal components of a wireless communication signal, the WTRU comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths, the digital HPFC module comprising:

a real signal input for receiving the real signal component;

a real compensated signal output for outputting a real compensated output signal;

a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

a first sample delay unit having an input and an output, the input of the first sample delay unit being connected to the output of the second adder;

a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the first sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module;

an imaginary signal input for receiving the imaginary signal component;

an imaginary compensated signal output for outputting an imaginary compensated output signal;

a third multiplier having first and second inputs and an output, the first input of the third multiplier for receiving the first compensation signal;

a fourth adder having first and second inputs and an output, the first input of the fourth adder being connected to the imaginary signal input of the digital HPFC module, and the output of the fourth adder being connected to the second input of the third multiplier;

a fifth adder having first and second inputs and an output, the first input of the fifth adder being connected to the output of the third multiplier;

a second sample delay unit having an input and an output, the input of the second sample delay unit being connected to the output of the second adder;

a fourth multiplier having first and second inputs and an output, the first input of the fourth multiplier for receiving the second compensation signal, the second input of the fourth multiplier being connected to the output of the second sample delay unit, to the second input of the fifth adder, and to the second input of the fourth adder; and

a sixth adder having first and second inputs and an output, the first input of the sixth adder being connected to the first input of the fourth adder, the second input of the sixth adder being connected to the output of the fourth multiplier, and the output of the sixth adder being connected to the imaginary compensated signal output of the digital HPFC module;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal path of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

Claim 14 (canceled)

15. (currently amended): The WTRU of claim 13 ~~claim 14~~ wherein a cutoff frequency, established by the analog real signal path HPF for the real signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

16. (currently amended): The WTRU of claim 13 ~~claim 14~~ wherein the gain of the high pass response of the real signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

17. (currently amended): The WTRU of claim 13 ~~claim 14~~ wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

18. (currently amended): The WTRU of claim 13 ~~claim 14~~ wherein the output of the first sample delay unit is subtracted from the real signal component via the first adder.

Claim 19 (canceled)

20. (currently amended): The WTRU of claim 13 ~~claim 19~~ wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

21. (currently amended): The WTRU of claim 13 ~~claim 19~~ wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

22. (currently amended): The WTRU of claim 13 ~~claim 19~~ wherein the output of the fourth ~~second~~ multiplier is subtracted from the imaginary signal component via the sixth ~~third~~ adder.

23. (currently amended): The WTRU of claim 13 ~~claim 19~~ wherein the output of the second sample delay unit is subtracted from the imaginary signal component via the fourth ~~first~~ adder.

24. (original): The WTRU of claim 13 wherein the digital HPFC module is selectively enabled or disabled.

25. (currently amended): An integrated circuit (IC) for adjusting a ~~the~~ frequency domain response of at least one of ~~the~~ real and imaginary signal components of a wireless communication signal, the IC comprising:

(a) a demodulator having real and imaginary signal outputs, the demodulator for receiving the communication signal and outputting real and imaginary signal components of the communication signal on the real and imaginary signal outputs;

(b) a digital high pass filter compensation (HPFC) module having real and imaginary signal paths, the digital HPFC module comprising:

a real signal input for receiving the real signal component;

a real compensated signal output for outputting a real compensated output signal;

a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital

HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

a first sample delay unit having an input and an output, the input of the first sample delay unit being connected to the output of the second adder;

a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the first sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module;

an imaginary signal input for receiving the imaginary signal component;

an imaginary compensated signal output for outputting an imaginary compensated output signal;

a third multiplier having first and second inputs and an output, the first input of the third multiplier for receiving the first compensation signal;

a fourth adder having first and second inputs and an output, the first input of the fourth adder being connected to the imaginary signal input of the digital HPFC module, and the output of the fourth adder being connected to the second input of the third multiplier;

a fifth adder having first and second inputs and an output, the first input of the fifth adder being connected to the output of the third multiplier;

a second sample delay unit having an input and an output, the input of the second sample delay unit being connected to the output of the second adder;

a fourth multiplier having first and second inputs and an output, the first input of the fourth multiplier for receiving the second compensation signal, the second input of the fourth multiplier being connected to the output of the second sample delay unit, to the second input of the fifth adder, and to the second input of the fourth adder; and

a sixth adder having first and second inputs and an output, the first input of the sixth adder being connected to the first input of the fourth adder, the second input of the sixth adder being connected to the output of the fourth multiplier, and the output of the sixth adder being connected to the imaginary compensated signal output of the digital HPFC module;

(c) at least one analog real signal path high pass filter (HPF) in communication with the real signal output of the demodulator and the real signal path of the digital HPFC module; and

(d) at least one analog imaginary signal path HPF in communication with the imaginary signal output of the demodulator and the imaginary signal path of the digital HPFC module, wherein the digital HPFC module suppresses group delay variation distortion caused by at least one of the analog real and imaginary HPFs.

Claim 26 (canceled)

27. (currently amended): The IC of claim 25 ~~claim 26~~ wherein a cutoff frequency, established by the analog real signal path HPF for the real signal

component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

28. (currently amended): The IC of claim 25 ~~claim 26~~ wherein the gain of the high pass response of the real signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

29. (currently amended): The IC of claim 25 ~~claim 26~~ wherein the output of the second multiplier is subtracted from the real signal component via the third adder.

30. (currently amended): The IC of claim 25 ~~claim 26~~ wherein the output of the first sample delay unit is subtracted from the real signal component via the first adder.

Claim 31 (canceled)

32. (currently amended): The IC of claim 25 ~~claim 31~~ wherein a cutoff frequency, established by the analog imaginary signal path HPF for the imaginary signal component frequency domain response, is reduced in response to adjusting the first predetermined value (K_1) of the first compensation signal.

33. (currently amended): The IC of claim 25 ~~claim 31~~ wherein the gain of the high pass response of the imaginary signal component frequency domain is controlled by adjusting the second predetermined value (K_2) of the second compensation signal.

34. (currently amended): The IC of claim 25 ~~claim 31~~ wherein the output of the fourth ~~second~~ multiplier is subtracted from the imaginary signal component via the sixth ~~third~~ adder.

35. (currently amended): The IC of claim 25 ~~claim 31~~ wherein the output of the second sample delay unit is subtracted from the imaginary signal component via the fourth ~~first~~ adder.

36. (original): The IC of claim 25 wherein the digital HPFC module is selectively enabled or disabled.

37. (new): A digital high pass filter compensation (HPFC) module having real and imaginary signal paths, the digital HPFC module comprising:

(a) a real signal input for receiving a real signal component of a wireless communication system;

(b) a real compensated signal output for outputting a real compensated output signal;

(c) a first multiplier having first and second inputs and an output, the first input of the first multiplier for receiving a first compensation signal having a first predetermined value (K_1);

(d) a first adder having first and second inputs and an output, the first input of the first adder being connected to the real signal input of the digital HPFC module, and the output of the first adder being connected to the second input of the first multiplier;

(e) a second adder having first and second inputs and an output, the first input of the second adder being connected to the output of the first multiplier;

(f) a first sample delay unit having an input and an output, the input of the first sample delay unit being connected to the output of the second adder;

(g) a second multiplier having first and second inputs and an output, the first input of the second multiplier for receiving a second compensation signal having a second predetermined value (K_2), the second input of the second multiplier being connected to the output of the first sample delay unit, to the second input of the second adder, and to the second input of the first adder; and

(h) a third adder having first and second inputs and an output, the first input of the third adder being connected to the first input of the first adder, the second input of the third adder being connected to the output of the second multiplier, and the output of the third adder being connected to the real compensated signal output of the digital HPFC module;

(i) an imaginary signal input for receiving an imaginary signal component of the wireless communication signal;

(j) an imaginary compensated signal output for outputting an imaginary compensated output signal;

(k) a third multiplier having first and second inputs and an output, the first input of the third multiplier for receiving the first compensation signal;

(l) a fourth adder having first and second inputs and an output, the first input of the fourth adder being connected to the imaginary signal input of the digital HPFC module, and the output of the fourth adder being connected to the second input of the third multiplier;

(m) a fifth adder having first and second inputs and an output, the first input of the fifth adder being connected to the output of the third multiplier;

(n) a second sample delay unit having an input and an output, the input of the second sample delay unit being connected to the output of the second adder;

(o) a fourth multiplier having first and second inputs and an output, the first input of the fourth multiplier for receiving the second compensation signal, the second input of the fourth multiplier being connected to the output of the second sample delay unit, to the second input of the fifth adder, and to the second input of the fourth adder; and

(p) a sixth adder having first and second inputs and an output, the first input of the sixth adder being connected to the first input of the fourth adder, the second input of the sixth adder being connected to the output of the fourth multiplier, and the output of the sixth adder being connected to the imaginary compensated signal output of the digital HPFC module.